REMARKS

Claims 1-30 pending. Claims 1-30 are rejected. Claims 29-30 have been amended. Claims 1, 15, 29 and 30 were rejected under 35 USC 102(b) as being anticipated by McCaslin, US Patent No. 4,999,798. Claims 2-14 and 16-28 were rejected under 35 USC 103(a) as being unpatentable over McCaslin in view of prior art allegedly admitted by Applicant.

Applicants believe that all pending claims should be allowed, for the reasons cited below.

Drawings

The Examiner objected to Figures 1A, 1B, 1C, 1D, 3A and 3B because they allegedly display only prior art and should be labeled accordingly. The mentioned figures have been resubmitted and have been amended in accordance with the Examiner's suggestions.

35 USC 101: Claims 29 and 30

The Examiner rejected claims 29 and 30 under 35 USC 101 because they are allegedly directed to non-statutory subject matter. Claims 29 and 30 refer to computer program products. The Examiner provided suggestions for amending claims 29-30, and the claims have been amended according to those suggestions.

35 USC 112: Claims 2, 5, 7, 9, 11, 18, 20 and 22

The Examiner rejected claims 2, 5, 7, 9, 11, 18, 20 and 22 because it is allegedly unclear whether the claims are intended to be independent of dependent claims. By way of example, claim 2 recites "a multi-channel numerically controlled oscillator comprising *the integrator of claim 1*." (Emphasis added.) The Examiner noted that the reciting of a 'multi-channel... oscillator" in claim 2 is not consistent with claim 1, which pertains to "a multi-channel integrator."

It is respectfully submitted that claim 2 is a valid dependent claim. MPEP 608.01(n) III states that "the test as to whether a claim is a proper dependent claim is that it shall include every limitation of the claim from which it depends (35 U.S.C. 112, fourth paragraph)." Claim 2 pertains to an oscillator, but it also includes every limitation of claim 1, as it recites "the

integrator of claim 1." The MPEP supports the validity of a dependent claim structured along the lines of claim 2. MPEP 608.01(n) III, for example, confirms the validity of a dependent method claim that is a method for producing a product recited in an earlier independent product claim.

Claims 5, 7, 9, 11, 18, 20 and 22 are all dependent claims that have formats similar to that of claim 2. In view of the foregoing, it is respectfully requested that the rejection of claims 2, 5, 7, 9, 11, 18, 20 and 22 under 35 USC 112 be withdrawn.

Claims 1, 26, 28 and 29

Claim 1 was rejected under 35 USC 102(b) as being anticipated by McCaslin.

McCaslin pertains to a transient-error free interpolating decimator. See Abstract of McCaslin. The decimator includes an integrator and differentiator, such as integrator 12 and differentiator 16 in Fig. 2 of McCaslin. McCaslin appears to describe an improved decimator, in part by combining a multiplexer circuit, differentiator 12, integrator 16, counter and bypass circuits in a novel manner, as indicated in Figure 2 of McCaslin. Taken separately, however, integrator 12 and differentiator 16 appear to be structured according to known designs. Hence, integrator 12 and differentiator 16 structurally do not appear very different from Figures 1C and 1D in the present application, which describe prior art integrator and differentiator sections. The present application, however, pertains to novel types of integrators and differentiators, examples of which are illustrated as integrator 424-1 in Figure 4B and differentiator 450-1 in Figure 4C. A comparison of integrator 12 of Figure 2 of McCaslin and integrator 424-1 of Figure 4B of the present application may prove helpful to the Examiner in clarifying differences between McCaslin and the present application.

Page 5 of the Office Action recites that integrator 12 of Figure 2 of McCaslin discloses claim 1. Applicants respectfully disagree, at least because the elements of integrator 12 appear to follow a different design from the one presented in claim 1.

More particularly, claim 1 pertains to an integrator comprising various elements, including an integrator input, a delay section, a feedback line and an adder. Claim 1 further recites that the delay section comprises a plurality of delay elements connected in series between

the delay section input and the delay section output. Claim 1 further recites an adder with an adder output. Claim 1 further recites that a feedback line connects the delay section output to an adder input and that the adder output is connected to the delay section input. Claim 1 also recites that the integrator input is connected to an adder input. Examples of such features may be found in integrator 424-1 of Figure 4B of the present application.

Integrator 12 of Figure 2 of McCaslin lacks the above features. Page 5 of the Office Action identifies the "delay section" of claim 1 with delay element 46 in Figure 2 of McCaslin, but such an identification does not agree with claim 1. Claim 1 requires that a "delay section" comprises a *plurality* of delay elements, not just one. Under similar logic, "delay section output" should not be identified with the output to delay element 46, as was asserted on page 5 of the Office Action, because the output to delay element 46 clearly is not an output to a *plurality* of delay elements.

If it is assumed for the sake of argument that a "delay section" cannot be identified as comprising delay element 46 of Figure 2 of McCaslin, but at least as comprising delay elements 46 and 50 (the next element in series with 46), it becomes clear that Figure 2 does not agree with claim 1. Claim 1, for example, requires "a feedback line connecting the delay section output to the second adder input." Claim 1 further requires that the "second adder input" is part of an adder whose first adder input is connected to the integrator input. The output to the "delay section" i.e. delay elements 46 *and* 50 in Figure 2 of McCaslin, could be assumed for the sake of argument to be the output of element 50. That output, however, is not connected via a feedback line to the input of the adder that also receives the integrator input (identified as input 14 of integrator 12 by page 5 of the Office Action) as an input.

For at least the reasons cited above, McCaslin does not teach claim 1. Therefore, it is respectfully submitted that claim 1 is patentable over the prior art of record.

The arguments presented above with respect to claim 1 apply to claims 26, 28 and 29. Claim 26 pertains to a decimator that incorporates N integrators, each with features paralleling those recited in claim 1. Claim 28 pertains to an oscillator incorporating an integrator with features paralleling those of claim 1. Claim 29 is a computer program product claim with features paralleling those of claim 1.

Claims 15, 26, 27 and 30

The arguments presented above with respect to claims 1, 26, 28 and 29 are analogous to the arguments presented in this section regarding claims 15, 27 and 30. Claim 15 pertains to a differentiator. Page 6 of the Office Action recites that claim 15 is disclosed by differentiator 16 of Figure 2 of McCaslin. Applicants disagree, at least because differentiator 16 lacks some of the elements of claim 15. An example implementation of claim 15 is illustrated in differentiator 450-1 of Figure 4C of the present application. To clarify the differences between claim 15 and the prior art, the Examiner may find it helpful to compare differentiator 450-1 with differentiator 16 of Figure 2 of McCaslin.

More particularly, claim 15 pertains to a differentiator comprising, among other elements, a differentiator input, a delay section, a feedforward line and a subtractor. Claim 15 further recites that the delay section comprises a plurality of delay elements connected in series between the delay section input and the delay section output. Claim 15 further recites that the delay section output is connected to the second subtractor input. Claim 15 further recites that a feedforward line connects a differentiator input to the first subtractor input. Examples of such features may be found in differentiator 450-1 of Figure 4C of the present application.

Differentiator 16 of Figure 2 of McCaslin lacks the above features. Page 6 of the Office Action identifies the "delay section" of claim 15 with delay element 70 in Figure 2 of McCaslin, but such an identification does not agree with claim 15. Claim 15 requires that a "delay section" comprises a *plurality* of delay elements, not just one. Under similar logic, "delay section output" should not be identified with the output to delay element 70 (page 6 of the Office Action identified element 56 as such, but presumably meant delay element 70) because the output to delay element 70 clearly is not an output to a *plurality* of delay elements.

If it is assumed for the sake of argument that a "delay section" cannot be identified as comprising delay element 70 of Figure 2 of McCaslin, but at least as comprising delay elements 70 and 74 (the next element in series with 70), it becomes clear that Figure 2 does not agree with claim 15. Claim 15, for example, requires "a feedforward line connecting the differentiator input to the first subtractor input." Claim 15 further requires that the delay section output is connected to the second subtractor input. The output to the "delay section" i.e. delay elements 70 *and* 74 in Figure 2 of McCaslin, could be assumed for the sake of argument to be the output of element 74.

Even under such assumptions, however, there is no feedforward line connecting the differentiator input (identified in the Office Action as the input to differentiator 16 in Figure 2, presumably meaning the lines extending from switches 15 and 17 and entering the dotted line box outlining differentiator 16) to the input of a subtractor that also receives the delay section output (i.e. output of element 74) as an input.

For at least the reasons cited above, it is respectfully submitted that claim 15 is patentable over the prior art of record.

The arguments presented above with respect to claim 15 apply to claims 26, 27 and 30. Claim 26 pertains to a decimator including N differentiators, each with features paralleling those recited in claim 15. Claim 27 pertains to a interpolator that incorporates N differentiators, each with features paralleling those recited in claim 15. Claim 30 is a computer program product claim with features paralleling those of claim 15.

The various dependent claims are respectfully submitted to be patentable over the art of record for at least the same reasons as set forth above with respect to their associated independent claims. Furthermore, these dependent claims recite additional features that when considered in the context of the claimed invention, further patentably distinguish the art of record.

Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, Applicants' attorney, Eric Yoon, can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. **ALTRP092**).

Respectfully submitted,
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